Af/2818

PATENT APPLICATION

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October 31, 2002 Kay Nutt
Kay Nutt

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	John R. Stice	Examiner:	Phan, Trong Q.
Appl. No.:	09/541,460	Art Unit:	2818
Filing Date:	March 31, 2000	Docket:	98-035

October 31, 2002

For: Analog to Digital Converter Utilizing Resolution Enhancement

Assistant Commissioner for Patents
Attention: Board of Patent Appeals and Interferences
Washington, DC 20231

BRIEF ON APPEAL

Sir:

Applicant files three copies of this Brief on Appeal within two months following filing a Notice of Appeal mailed July 23, 2002 and received in the Patent Office August 2, 2002. Please charge the fee of $320.00 under 37 C.F.R. §1.17(f) to Deposit Account No. 02-2960. The Applicant petitions the Commissioner of Patents and Trademarks to extend the time for for filing this Brief on Appeal for one month from October 2, 1001 to November 2, 2002.

Please charge the fee of $110.00 to Deposit Account No. 02-2960. Please charge any necessary additional fees under 37 C.F.R. § 1.16 or § 1.17 or credit any overpayments to Deposit Account No. 02-2960.

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02 FC:1251 110.00 CH

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is The Boeing Company.

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II. RELATED APPEALS AND INTERFERENCES

Applicant does not know of any other appeals or interferences that directly affect or will be directly affected by the Board's decision in this appeal.

III. STATUS OF CLAIMS

1. Claims pending: 1 - 8
2. Claims canceled: Claim 3
3. Claims withdrawn from consideration but not canceled: 8 - 10
4. Claims allowed: Claim 6
5. Claims rejected: Claims 1-5, 7 and 8
6. Claims on appeal: 1, 2, 4, 5, 7 and 8

IV. STATUS OF AMENDMENTS

Applicant filed an Amendment After Final Rejection mailed May 13, 2001, which does not appear to have been acted upon by the Examiner.

V. SUMMARY OF INVENTION

A brief summary of the invention (found at p. 6, line 17 to p. 7, line 7.

The present AD converter system concerns those signals, which have a low frequency component (such as DC) superimposed upon an AC component. The magnitude of the AC component must be less than or equal to one-half the span of the converter. The majority of signal transducers, such as pressure to voltage converters, satisfy this requirement. For these signals, the present invention provides a high resolution ADC with the simplicity advantage inherent in a reduced resolution ADC. This is accomplished by first connecting the input signal through a programmed gain preamplifier. The preamplifier matches the full range of the ADC to only the AC component portion of the input signal. In order to cover the entire input signal, the ADC's range is complemented by an offset value. The advantage of this technique is the

preamplifier, designed to amplify the input signal at high gain, while applying the offset value at low gain. A digital summing junction combines the analog to digital conversion results with the offset value, resulting in a higher precision overall conversion.

VI. ISSUES

Whether the drawings show the features specified in the claims, viz. the converter of line 2 of claim 5, the hysteresis in line 6 of claim 7, and the AD converter performing the method of claim 8.

Whether claims 7-8 are clear within the meaning of 35 U.S.C. 112, first paragraph, more particularly the relationship of overlapping offset bands to hysteresis and whether method claim 8 is sufficiently described in the specification for the understanding of one skilled in the art.

Whether applicant's amendments to independent claims 1, 4, 7 and 8 in the form shown in applicant's "Amendment After Final Rejection" render said claims definite within the meaning of 35 U.S.C. 112, second paragraph.

Whether claim 3 is patentable over Katsumata et al. ('189) within the meaning of 35 U.S.C. 103(a).

Claim 6 is not an issue in this appeal since currently being rewritten in independent form and filed in a continuation application.

VII. GROUPING OF CLAIMS

Since each of appealed claimsn1, 2, 4, 5, 7 and 8 stand separately rejected for indefiniteness under 35 U.S.C. 112, they are not grouped together for consideration in this appeal.

VIII. ARGUMENTS (35 U.S.C. 112)

(Rejections other than 35 U.S.C., 102, 103)

Responsive to VI Issues

I. Drawings:

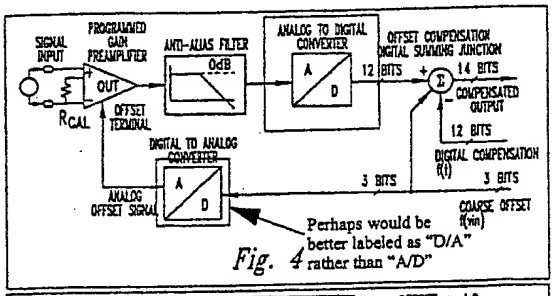

Fig. 4

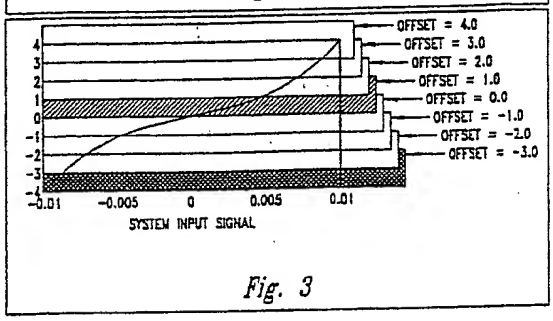

Fig. 3

The analog to digital converter is the top block labeled "A/D" in Fig. 4 and the hysteresis referred to is a mathematical operation shown schematically by Fig. 3. There is not a dedicated hardware item which performs the hysteresis function. Hysteresis is applied as part of the coarse offset which originates as part of the device's digital controls. Note that in Fig. 4 there are three bits controlling coarse offset. These three bits correspond to the eight levels of offset illustrated in figure3, since $2^3 = 8$ as originally discussed in the patent application's opening remarks.

Figure 4 shows two blocks labeled "A/D." Customarily, "A/D" refers to an analog to digital conversion function. One of the blocks shown in figure 4 is in reality a digital to analog converter, customarily referred to as "D/A." This typographical error is possibly confusing to those seeing the figure for the first time.

By way of further explanation, the hysteresis function is provided for those situations in which the signal being processed is just on the edge of transitioning from one offset range into an adjacent offset range: Suppose hysteresis was not provided. The offset ranges would not overlap

as shown in figure 3, but would rather abut one another. In this case, should a signal make a transition from one offset range into the adjacent offset range and then for whatever reason quickly transition back into its original offset range (which could easily be the case for a signal "hovering" close to a range boundary), an undesirable effect of continuously switching ranges could occur. Providing hysteresis in which offset ranges overlap as shown in figure 3 eliminates this effect. Once the signal transitions into an adjacent offset range, it finds itself in the middle of this new range rather than on the range's edge as would be the case if hysteresis were not provided.

II and III - Claim Rejections – 35 U.S.C 112

Examiner's Comment:
Claims 7-8 contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 7 recounts the offset bands shown vertically displaced along figure 3's vertical axis. Claim 8 summarizes the operation of the overall circuit: Resolution of this conversion scheme is enhanced by digitizing an input signal from which a DC component is subtracted. The numeric value of that DC component is then mathematically summed back in to the converted result which has the effect of increasing the apparent number of conversion bits.

Examiner's Comment:
It is not clear how overlapping the offset bands can provide the hysteresis as recited in line 6 of claim 7 since Fig. 3 of the present invention does not show any analog to digital converter and the hysteresis in combination with the offset bands.

Again, the basic idea behind hysteresis is that once an input signal transitions into an adjacent offset range, it finds itself in the middle of this new range rather than on the range's edge as would be the case if the ranges abutted rather than overlapped. Hysteresis prevents a signal from leaving an offset range until it crosses that range's boundary. Once it crosses a range boundary,

it then finds itself in the middle of the adjacent range so that it cannot immediately return to the range from which it started. This presents continuous, undesirable range changes.

Examiner's Comment:
The method as recited in claim 8 is not described under detailed description of the invention of the present specification. It is just briefly described under Patent Literature from line 7 to line 18 of page 5 of the present specification.

Claim 8 is a summary of the proposed invention. Please see the remarks in the preceding paragraph.
Claims 1-2, 4-5, and 7-8 were indicated as indefinite in paragraph 5 of the Office Letter. Accordingly, the objections are believed addressed in the claims as now amended.

Further Response:
First, the word "span" in this context refers to the range of voltages which can be accommodated by the analog to digital converter block labeled "A/D" shown in Fig. 4. This "A/D" block must be distinguished from the digital to analog converter block unfortunately also labeled "A/D". The mark-ups on the above figures, hereby made of record, should clarify which is which.

Claims 1 and 2 describe the process of the circuit adapting itself to the particular transducer to which it is connected. For transducers having a relatively large output signal, the input preamplifier need have only relatively small gain to match the transducer output to the analog to digital converter block's span. Conversely, for transducers having a relatively small output signal, the input preamplifier need have a relatively large gain to match the transducer output to the analog to digital converter block's span.

Claims 4 and 5 identify the blocks shown in Fig. 4.
Claims 7 and 8 summarize the circuit's operation.

IV. - Claim Rejections 35 U.S.C. 103 (paragraph 7 of the Office Letter)

Claim 3 has been cancelled without prejudice.

Allowable Subject Matter

Claim 6 was indicated as allowable subject to being rewritten in independent form, which is accomplished in a separately filed continuing application.

CONCLUSION

Applicant believes the drawings to be a very complete representation of the invention as claimed and that claims 1, 2, 4, 5, 7 and 8 as currently presented and as previously amended in the "Amendment After Final Rejection" in response to 35 U.S.C. 112 obviate the concerns of the Examiner in this regard.

For the reasons given above, it is believed this application is in condition for allowance.

Respectfully submitted,

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IX. APPENDIX

The appealed claims are:

1. An analog to digital converter resolution enhancement method comprising the steps of:

providing an analog to digital converter having an AC component less than or equal to one-half the full range of signals which the analog to digital converter itself can accommodate;

connecting the input signal to the input of a programmed gain preamplifier;

utilizing said programmed gain preamplifier to match the full range of said analog to digital converter to said AC component of the input signal; and then,

enhancing the analog to digital conversion range of said analog to digital converter by an offset value thereby causing said programmed gain preamplifier to amplify the input signal at high gain while applying the offset value at low gain.

2. An analog to digital converter having resolution enhancement comprising in combination:

an analog to digital converter having a full range and an input terminal and an output terminal;

a programmed gain preamplifier having an input terminal for receiving an input signal having an AC component portion and an output terminal coupled to the input terminal of said analog to digital converter;

said programmed gain preamplifier matching said full range of said analog to digital converter to only said AC component portion of the input signal;

said analog to digital converter having a range complemented by an offset value; and

a summing junction for combining the output of said analog to digital converter with said offset value thereby causing said programmed gain preamplifier to amplify the input signal at high gain while applying the offset value at low gain.

4. In combination:

a reduced span analog to digital converter;

a programmed gain preamplifier coupled between an input terminal for receiving an input signal and said reduced span analog to digital converter;

said programmed gain preamplifier having a high differential gain for said input signal and a low single-ended gain for the offset signal;

said programmed gain preamplifier matching the range of signals which said analog to digital converter can fully accommodate against only a portion of the signal present at the circuit's input; and,

the entire range of signals provided by positioning the analog to digital converter's input signal range by means of an offset value.

5. In combination:

an analog to digital converter having an input terminal and an output terminal;

a programmed gain preamplifier having an input terminal for receiving an input signal, an offset terminal, and an output terminal;

a digital summing junction;

said output terminal of said analog to digital converter coupled to said digital summing junction;

an anti-alias filter having an input terminal and an output terminal;

said output terminal of said anti-alias filter coupled to said input of said analog to digital converter;

said input terminal of said anti-alias filter coupled to said output terminal of said programmed gain preamplifier; and,

said digital to analog converter coupled between said digital summing junction and said offset terminal of said programmed gain preamplifier for providing an analog offset signal to said programmed gain preamplifier.

7. In the method of operating an analog to digital converter for resolution enhancement, the steps of:

displacing the input signal range of the analog to digital converter to one of a plurality of overlapping positions comprising offset bands wherein the width of each band is representative of the input signal range of the analog to digital converter; and,

overlapping the offset positions to provide hysteresis.

8. A method for resolution enhancement in an analog to digital converter comprising the steps of:

converting a reference voltage of more than a least significant bit;

subtracting a mathematically-derived reference voltage of more than a least significant bit from the circuit's input voltage; and then

adding the converted reference voltage of more than a least significant bit to the converted reduced input voltage.